What is claimed is:

1. A method of fabricating a memory cell array in which memory cells formed of ferroelectric capacitors are arranged in a matrix, comprising the steps of:

forming a first signal electrode with a predetermined pattern on a base;

selectively forming a ferroelectric layer on the first signal electrode linearly along the first signal electrode; and

forming a second signal electrode in a direction intersecting the first signal electrode.

2. The method of fabricating a memory cell array as defined in claim 1, further comprising the steps of:

forming on the base a first region having surface properties which give priority in deposition to a material of at least one of the first signal electrode and the ferroelectric layer, and a second region having surface properties which give difficulty in deposition to the material of at least one of the first signal electrode and the ferroelectric layer in comparison with the first region; and

providing the material of at least one of the first signal electrode and the ferroelectric layer and selectively forming one of the first signal electrode and the ferroelectric layer in the first region.

3. The method of fabricating a memory cell array as defined

in claim 2,

wherein the first and second regions are defined on a surface of the base.

4. The method of fabricating a memory cell array as defined in claim 3, wherein:

the surface of the base is exposed in the first region; and

in the second region is formed an undercoat layer having surface properties having a low affinity for materials of the first signal electrode and the ferroelectric layer in comparison with the exposed surface of the base in the first region.

5. The method of fabricating a memory cell array as defined in claim 3, wherein:

the surface of the base is exposed in the second region; and

in the first region is formed an undercoat layer having surface properties having a high affinity for materials of the first signal electrode and the ferroelectric layer in comparison with the exposed surface of the base in the second region.

6. The method of fabricating a memory cell array as defined in claim 1,

wherein a dielectric layer is provided between laminates each of which includes the first signal electrode and the ferroelectric layer so as to cover an exposed surface of the

base.

7. The method of fabricating a memory cell array as defined in claim 6,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

8. A method of fabricating a memory cell array in which memory cells formed of ferroelectric capacitors are arranged in a matrix, comprising the steps of:

forming a first signal electrode with a predetermined pattern on a base; and

forming a ferroelectric layer and a second signal electrode in a direction intersecting the first signal electrode, wherein the ferroelectric layer is disposed linearly along the second signal electrode.

9. The method of fabricating a memory cell array as defined in claim 8,

wherein the ferroelectric layer and the second signal electrode are patterned by etching using the same mask.

10. The method of fabricating a memory cell array as defined in claim 8,

wherein a dielectric layer is provided between laminates each of which includes the second signal electrode and the

ferroelectric layer so as to cover an exposed surface of the base and an exposed surface of the first signal electrode.

11. The method of fabricating a memory cell array as defined in claim 10,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

12. A method of fabricating a memory cell array in which memory cells formed of ferroelectric capacitors are arranged in a matrix, comprising the steps of:

forming a first signal electrode with a predetermined pattern on a base;

forming a ferroelectric layer on the first signal electrode linearly along the first signal electrode;

forming a second signal electrode in a direction intersecting the first signal electrode; and

patterning the ferroelectric layer to be disposed only in an intersection area of the first and second signal electrodes.

13. The method of fabricating a memory cell array as defined in claim 12, further comprising the steps of:

forming on the base a first region having surface properties which give priority in deposition to a material of at least one of the first signal electrode and the ferroelectric layer, and a second region having surface properties which give

difficulty in deposition to the material of at least one of the first signal electrode and the ferroelectric layer in comparison with the first region; and

providing the material of at least one of the first signal electrode and the ferroelectric layer and selectively forming one of the first signal electrode and the ferroelectric layer in the first region.

14. The method of fabricating a memory cell array as defined in claim 13,

wherein the first and second regions are formed on a surface of the base.

15. The method of fabricating a memory cell array as defined in claim 14, wherein:

part of the surface of the base is exposed in the first region; and

in the second region is formed an undercoat layer having surface properties having a low affinity for materials of the first signal electrode and the ferroelectric layer in comparison with the exposed surface of the base in the first region.

16. The method of fabricating a memory cell array as defined in claim 14, wherein:

part of the surface of the base is exposed in the second region; and

in the first region is formed an undercoat layer having

surface properties having a high affinity for materials of the first signal electrode and the ferroelectric layer in comparison with the exposed surface of the base in the second region.

17. The method of fabricating a memory cell array as defined in claim 12,

wherein the ferroelectric layer and the second signal electrode are patterned by etching using the same mask.

18. The method of fabricating a memory cell array as defined in claim 12,

wherein a dielectric layer is provided between laminates each of which includes the first signal electrode and the ferroelectric layer so as to cover an exposed surface of the base.

19. The method of fabricating a memory cell array as defined in claim 18,

wherein the dielectric layer is provided between laminates each of which includes the second signal electrode and the ferroelectric layer so as to cover the exposed surface of the base and an exposed surface of the first signal electrode.

20. The method of fabricating a memory cell array as defined in claim 19,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.